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EXAMINER	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/522,007	KIM, JONG-SEON	
	Examiner	Art Unit	
	Michael Pervan	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 October 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,4-8 and 10-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4-8 and 10-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 January 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed October 1, 2009 have been fully considered but they are not persuasive.

Applicant (on pages 5-6 of argument) argues that Knapp and Iida do not disclose simultaneous sequential scanning of first and third gate lines. Examiner respectfully disagrees.

Knapp discloses sequential scanning of the gate lines 1-M (paragraphs 15 and 21). While Iida discloses simultaneous scanning of a first (top gate lines) area and a third area (bottom gate lines). If this method of simultaneously scanning the top and the bottom gate lines of Iida was applied to the sequential scanning of the gates lines of Knapp, one would arrive at the claimed invention, e.g., Knapp would simultaneously scan the top and bottom gate lines in a sequential manner. Therefore, Knapp and Iida still read on the claims and the rejection stands.

Applicant (on pages 6-7 of argument) argues that Knapp does not disclose providing the same data voltages to pairs of data lines while second areas are scanned and that the two circuits do not apply voltages at the same time. Examiner respectfully disagrees.

Knapp discloses that the driver circuits (35A, 35B) receive video information from an input video signal (data voltages) from the timing and input control unit (40) via respective supply busses (37A, 37B) (paragraph 22). Therefore, Knapp applies the

same data voltage to both pairs of data lines while the second area is scanned. Also, Knapp discloses that the total field period for which both circuits are operating simultaneously is small (lines 14-16 of paragraph 29). Since the circuits are operating at the same time, however brief it may be, the voltages would be applied to the pairs of data lines while the second area is scanned. As a result, Knapp still reads on the claims and the rejection stands.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 4-5, 8 and 10-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Knapp in view of Iida et al (US 6,236,388).

In regards to claim 1, Knapp discloses a liquid crystal display, comprising:

a plurality of first, second, and third gate lines (Fig. 3 and paragraphs 27-28; as can be seen in the drawing, the gate lines (rows) are divided into three groups 1~K, K~K+X and K+X~M) transmitting scanning signals provided on a first, a second, and a third area, respectively;

a plurality of pairs of first and second data lines transmitting data voltages (Fig. 3 and paragraph 20; pairs of first and second data lines (columns)), each pair having its

first and second data lines separated from each other at a disconnecting points (break) (Fig. 3 and paragraphs 20 and 27); and

a plurality of pixels connected to at least one of the gate lines and at least one of the data lines and arranged in a matrix, the pixels including a plurality of first, second, and third pixels provided on the first, the second, and the third areas, respectively (Fig. 3 and paragraph 19),

wherein the disconnecting points of the pairs of first and second data lines are randomly distributed on the second area (Fig. 3 and paragraphs 27-28; disconnections (breaks) are randomly distributed;

wherein the first, second and third gate lines are parallel to one another (fig. 3; as can be seen from the drawing, the first, second and third gate lines are parallel to one another); and

wherein same data voltages are provided on the data lines of each pair while the respective gate lines are scanned (paragraph 29).

Knapp does not disclose wherein the first gate lines are sequentially scanned while the third gate lines are sequentially scanned, after which the second gate lines are sequentially scanned.

Iida discloses a scanning method of scanning the upper-side rows and lower-side rows simultaneously with a black signal, and then scans the rows with a black and an image signal (Figs. 4-5 and col. 9, line 55-col. 10, line 17). If this scanning method were applied to Knapp, the claimed limitation would be met because the first gate line in the first area and the first gate line in the third area are scanned simultaneously, then the

second gate line in the first area and the second gate line in the third area are scanned simultaneously and so on until the gate lines in the second area are scanned. Therefore, the first and third gate lines are scanned simultaneously and the second gate lines are scanned after the first and the third gate lines.

It would have been obvious at the time of invention to modify Knapp with the teachings of Iida, displaying multiple image resolutions, because it reduces the amount of signal processing required by the driver, thus reducing power consumption.

In regards to claim 3, Knapp discloses the liquid crystal display of claim 1, wherein each pair of first and second data lines are supplied with a single data voltage during the scanning of each of the second gate lines (paragraph 29).

In regards to claim 4, Knapp discloses the liquid crystal display of claim 1, wherein the number of the first gate lines is equal to the number of the third gate lines, and the second area is disposed between the first area and the third area (Fig. 3 and paragraph 28).

In regards to claim 5, Knapp discloses the liquid crystal display of claim 4, wherein the scanning directions for the first, the second, and the third gate lines are the same (paragraph 21; since the scanning is successive from row 1~M the direction is the same for the first, the second and the third gate lines).

In regards to claim 8, Knapp discloses the liquid crystal display of claim 6, wherein the image data for the first pixels and the third pixels are supplied to the first data driver and the second data driver, respectively, and the image data for the second pixels are supplied to both the first and the second data drivers (paragraphs 22 and 29).

In regards to claim 10, Knapp discloses the liquid crystal display of claim 6, wherein the number of the first gate lines is equal to the number of the third gate lines, and the second area is disposed between the first area and the third area (Fig. 3 and paragraph 28).

In regards to claim 11, Knapp discloses the liquid crystal display of claim 10, wherein the scanning directions for the first, the second, and the third gate lines are the same (paragraph 21; since the scanning is successive from row 1~M the direction is the same for the first, the second and the third gate lines).

In regards to claim 12, Knapp discloses a method of driving a liquid crystal display including a plurality of first, second, and third gate lines (Fig. 3 and paragraphs 27-28; as can be seen in the drawing, the gate lines (rows) are divided into three groups 1~K, K~K+X and K+X~M) transmitting scanning signals provided on a first, a second, and a third area, respectively, a plurality of pairs of first and second data lines, the data lines of each pair transmitting data voltages (Fig. 3 and paragraph 20; pairs of first and second data lines (columns)) and separated from each other at a disconnecting point

(break) (Fig. 3 and paragraphs 20 and 27-8), and a plurality of pixels connected to at least one of the gate lines and at least one of the data lines and arranged in a matrix, the pixels including a plurality of first, second, and third pixels provided on the first, the second, and the third areas, respectively (Fig. 3 and paragraph 19), the method comprising;

applying data voltages for each first pixel and each third pixel to the respective first data lines and second data lines (paragraphs 22 and 29); and

applying same data voltages for each second pixel to both the respective first and second data lines (paragraphs 22 and 29).

Knapp does not disclose the first gate lines being sequentially scanned while the third gate lines are sequentially scanned, after which the second gate lines are sequentially scanned, the method comprising:

sequentially applying scanning signals to the first gate lines while the third gate lines are sequentially scanned; and

after the applying data voltages for each first pixel and each third pixel, sequentially applying scanning signals to the second gate lines.

Iida discloses a scanning method of scanning the upper-side rows and lower-side rows simultaneously with a black signal, and then scans the rows with a black and an image signal (Figs. 4-5 and col. 9, line 55-col. 10, line 17). If this scanning method were applied to Knapp, the claimed limitation would be met because the first gate line in the first area and the first gate line in the third area are scanned simultaneously, then the second gate line in the first area and the second gate line in the third area are scanned

simultaneously and so on until the gate lines in the second area are scanned. Therefore, the first and third gate lines are scanned simultaneously and the second gate lines are scanned after the first and the third gate lines.

It would have been obvious at the time of invention to modify Knapp with the teachings of Iida, displaying multiple image resolutions, because it reduces the amount of signal processing required by the driver, thus reducing power consumption.

In regards to claim 13, Knapp does not disclose the method of claim 12, wherein the application of scanning signals to the second gate lines is performed after the application of scanning signals to the first gate lines and the third gate lines.

Iida discloses the method of claim 12, wherein the application of scanning signals to the second gate lines is performed after the application of scanning signals to the first gate lines and the third gate lines (Figs. 4-5 and col. 9, line 55-col. 10, line 17; since the upper and lower-sides are scanned with a black signal and then the rows are scanned with a black and an image signal, the first and third gate lines would be scanned at the same time and prior to the second scan lines.).

It would have been obvious at the time of invention to modify Knapp with the teachings of Iida, displaying multiple image resolutions, because it reduces the amount of signal processing required by the driver, thus reducing power consumption.

4. Claims 6-7 and 14-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Knapp in view of Iida et al in further view of Park et al (JP 2000-310767; US 7,136,040 is used as a translation only).

In regards to claim 6, Knapp discloses the liquid crystal display of claim 1, further comprising:

first and second data drivers (column drivers 35A, 35B) applying the data voltages to the first and the second data lines, respectively (paragraph 29);

a gate driver (row driver circuit 30) applying the scanning signals to the first, the second, and the third gate lines (paragraph 21).

Knapp and Iida do not disclose a memory storing image data corresponding to the data voltages and supplying the image data to the first and the second data drivers.

Park discloses a memory storing image data corresponding to the data voltages and supplying the image data to the first and the second data drivers (col. 7, lines 58-63).

It would have been obvious at the time of invention to modify Knapp and Iida with the teachings of Park, memory storing image data and supplying the image data to first and second data drivers, because the memory acts as a buffer, which improves prevention of data loss.

In regards to claim 7, Knapp and Iida do not disclose the liquid crystal display of claim 6, wherein the image data are written in the memory in synchronization with a

write dock and are read in synchronization with a read dock having a frequency substantially half of a frequency of the write clock.

Park discloses the liquid crystal display of claim 6, wherein the image data are written in the memory in synchronization with a write dock and are read in synchronization with a read dock having a frequency substantially half of a frequency of the write clock (col. 8, lines 2-8).

It would have been obvious at the time of invention to modify Knapp and Iida with the teachings of Park, read clock with half the frequency of the write clock, because it ensures that all the data in memory is read out and written to the display.

In regards to claim 14, Knapp and Iida do not disclose the method of claim 12, further comprising:

writing image signals corresponding to the data voltages into a memory in synchronization with a write clock;

reading out the image signals for the first and the third pixels in synchronization with a read clock;

converting the read-out image signals for the first and the third pixels into the data voltages;

reading out the image signals for the second pixels in synchronization with the read clock; and

converting the read-out image signals for the second pixels into the data voltages.

Park discloses the method of claim 12, further comprising:

writing image signals corresponding to the data voltages into a memory in synchronization with a write clock (col. 8, lines 21-36);

reading out the image signals for the first and the third pixels in synchronization with a read clock (col. 8, lines 37-51);

converting the read-out image signals for the first and the third pixels into the data voltages (col. 8, lines 52-58);

reading out the image signals for the second pixels in synchronization with the read clock (col. 8, lines 37-51); and

converting the read-out image signals for the second pixels into the data voltages (col. 8, lines 52-58).

It would have been obvious at the time of invention to modify Knapp and Iida with the teachings of Park, writing image data, reading image data and converting image data, because it is a conventional method of applying image data to pixels to produce an image on the display.

In regards to claim 15, Knapp and Iida do not disclose the method of claim 14, wherein the read clock has a frequency substantially equal to half of a frequency of the write clock.

Park discloses the method of claim 14, wherein the read clock has a frequency substantially equal to half of a frequency of the write clock (col. 8, lines 2-14).

It would have been obvious at the time of invention to modify Knapp and Iida with the teachings of Park, read clock with half the frequency of the write clock, because it ensures that all the data in memory is read out and written to the display.

Conclusion

5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael Pervan whose telephone number is (571) 272-0910. The examiner can normally be reached on Monday - Friday between 8am - 5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amr Awad can be reached on (571) 272-7764. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

MVP

/Amr Awad/
Supervisory Patent Examiner, Art Unit 2629

Dec. 29, 2009